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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/537,563	06/03/2005	Hisaharu Nakahara	NAA218	4547

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GALLAGHER & LATHROP, A PROFESSIONAL CORPORATION
601 CALIFORNIA ST
SUITE 1111
SAN FRANCISCO, CA 94108

EXAMINER	
NATALINI, JEFF WILLIAM	
ART UNIT	**PAPER NUMBER**
2858	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/537,563	NAKAHARA, HISAHARU	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2007*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *4-6,8 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL ACTION

Drawings

1. Figures 1a, 1b, 1c, and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 3 and 7 are objected to because of the following informalities:

In regard to claim 3, lines 9-11 the wording "as the voltages to be measured the potential difference there between" seems to have improper grammar and should be replaced with "to measure a potential difference there between".

In regard to claim 7, the claim states that both the inverted and non-inverted terminals are connected to ground, but surely this is incorrect based on the figures and the pre-amended claim. It seems the claim should be changed to state "said operational amplifier has inverted and non-inverted terminals, wherein the non-inverted terminal is connected to ground" and the claim will be examined as such.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto (6255842).

In regard to claim 1, Hashimoto discloses a voltage impressed current measuring apparatus which impresses a prescribed voltage and measures a current flowing in a load apparatus (abstract) comprising:

a current range switching portion having a plurality of series connections (figure 1 connections b, c, and d represent each series connections midpoint), each comprising a current buffer with a switch connected in series with a current measurement resistance (series connection 1 (SC1) is elements 12A, R3, S5; SC2 is elements 12A, R3 in series with R2, and S6; SC3 is elements 12A, R3-R2-R1 in series, and S7) wherein each of the current buffers with switches has an output stage capable of being electrically connected or disconnected (elements S5-S7 are able to connect and disconnect the particular series connection) and a pre-stage portion controlling the output stage in its connected or disconnected state in response to a control signal supplied thereto and capable of acting as a current buffer (12B, the control signal is based on what switch is on, see figure 2, which would control the output stage; also 12B and 12A can be

considered pre-stage, since the buffer in the present applications' drawings is both part of pre-stage and the series connection), the current measurement resistances have different resistance values and one end of a measurement resistance connect to the output stage of it's respective current buffer with a switch and the other end connects to the output side of the respective series connection connected to the load apparatus (series connections 1-3 as described above and the load is element 11), and the control signal selects any one of the plurality of series connections to switch the current measurement range so that the output stage of the current buffer with a switch of the selected series connection is taken to be in its connected state (figure 2, Sp1-Sp4);

a direct-current power supply portion, connected to input ends of the pre-stage portions as input sides of the respective series connects and supplying the prescribed direct-current voltage to the load apparatus through the selected series connection (a voltage is applied to the DA converter element 12B (the arrow coming into 12B) so it is able to supply a voltage to the IC under test, see col 1 line 38-43); and

a potential difference measuring means, measuring, as a value corresponding to the current flowing in the load apparatus, due to the impression of the direct-current voltage on the load apparatus, a potential difference between the input side of the output side of the selected series connection due to the current which flows from the current buffer with a switch of the selected series connection to the load apparatus (col 3 line 43-64).

In regard to claim 2, Hashimoto discloses wherein a digital to analog converter which converts a digital voltage supplied to an input end thereof to an analog reference

voltage (figure 1 element 12), and an operation amplifier (figure 1 element 12A) to which the reference voltage is applied and which is controlled by feedback of the voltage impressed on the load apparatus (figure 11) so that an output voltage thereof is supplied to the load apparatus via the range switching portion (figure 1, the voltage applied to the load is fed back to one of the inputs of the operational amplifier).

In regard to claim 10, Hashimoto discloses wherein the output sides of the plurality of series connections connect to a single terminal of a device under test (figure 3- point labeled SEN, into one terminal of load element 11).

5. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hashimoto (6255842) in view of Hirofumi (JP 63-082377 on IDS).

Hashimoto discloses

(claim 3) a voltage at the input side of the current buffers with switches and a voltage at the output side of the current measurement resistances of the selected series connection are supplied to the potential difference measuring portion as the voltages to be measured the potential difference there between (col 3 line 43-64).

(claim 7) wherein the operational amplifier has a non-inverting and inverting input terminals (figure 1 element 12A)

Hashimoto lacks specifically

(claim 3) wherein the input sides of the plurality of current buffers (a plurality of current buffers is not needed in the broad interpretation of claim 1 as seen in the rejection above, wherein by using switches each series connection has a current buffer,

but they just happen to be the same current buffer in different series connections based on which switches are opened/closed) are connected to the output side of the operational amplifier.

(claim 7) wherein the non-inverter input of said operational amplifier is connected to ground, and the current power supply portion comprises a first resistance inserted between an output of the digital to analog converter and the inverted input terminal of the operational amplifier, and a second resistance inserted in the feedback path from the load apparatus to the inverted input of said operational amplifier.

Hirofumi discloses

(claim 3) a current measuring circuit wherein a current buffer (figure 1 element 16) and switches (figure 1 Ry1-Ryn) are connected to the output side of the operation amplifier (fig 1 element 14),

(claim 7) wherein said current power supply portion comprises a first resistance (fig 1 element 20) inserted between the output of the digital to analog converter (fig 1 element 16) and the inverted input of the operational amplifier (fig 1 element 14), and a second resistance (fig 1 element 24) inserted in the feedback path from the load apparatus (fig 1 element 10) to the inverted input terminal of the operational amplifier (fig 1 element 14), and the non-inverter input terminal of the operational amplifier is connected to ground (fig 1 element 14 has non-inverted input connected to ground).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Hashimoto to include an operational amplifier having an output side connected to an input of a buffer element and switches, wherein the non-inverted

terminal is connected to ground, and a second resistance is included in the feedback path is connected to the inverted input terminal as taught by Hirofumi in order to provide a quick current measurement (see purpose in English abstract).

Response to Arguments

6. Applicant's arguments with respect to claims 1-3, 7, and 10 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tanase (5414352) discloses a parametric test circuit, that has

series connections of resistors and switches into a terminal of a load. West (6940271) discloses a pin electronics test that includes multiple buffers and switches with a resistance in series.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Hirshfeld can be reached on 571-272-2168. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeff Natalini

Walter Benson
WALTER BENSON, PHD, P.E.
PRIMARY EXAMINER